R E M A R K S

Careful review and examination of the subject application are noted and appreciated. Applicant thanks Examiner Bae for the indication of allowable matter in the previously presented claim 15. Currently amended claim 15 has a different scope.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments may be found in the specification, for example, on page 18 lines 3-9 and FIG. 4, as originally filed, and claims 12, 13, 14 and 15 prior to the instant amendment. Thus, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 16-20 under 35 U.S.C. 112, second paragraph, has been obviated by amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1-11 under 35 U.S.C. §103(a) as being unpatentable over Dorst '416 in view of Keskar et al. '989 (hereafter Keskar) has been obviated by amendment and should be withdrawn.

The rejection of claim 12 under 35 U.S.C. §103(a) as being unpatentable over Dorst and Keskar in further view of

Ghaffari '932 has been obviated by amendment and should be withdrawn.

The rejection of claims 13, 14 and 21 under 35 U.S.C. §103(a) as being unpatentable over Dorst, Keskar, and Ghaffari in further view of Cheng et al, '689 (hereafter Cheng) has been obviated by amendment and should be withdrawn.

Dorst teaches an apparatus and methods for dedicated command port in memory controllers (Title). Keskar teaches a programmable memory controller (Title). Ghaffari teaches a method and apparatus for increasing the performance of communications between a host processor and a SATA or ATA device (Title). Cheng teaches a method and apparatus for pre-caching data in audio memory (Title).

Claim 1 provides an interface circuit having a completion bit that indicates in alternate states that (a) a processor is finished with a current transfer to the interface circuit and (b) the interface circuit is ready to begin a new operation. In contrast, the busy bit of Cheng (used in rejecting similar language in former claim 13) appears to indicate the status of a DMA controller of Cheng, not the status of a memory interface type of circuit in communication with the DMA controller. Furthermore, the DMA controller of Cheng being ready for a new operation does not mean that a memory interface type of circuit is also ready for a new operation. The specification of the instant application

provides and example on page 18, lines 3-9 where the filling and draining of a FIFO in the memory interface causes the memory interface to lag behind the initiating host (such as a DMA engine) in the processor. Therefore, Dorst, Keskar, Ghaffari and Cheng, alone or in combination, do not appear to teach or suggest an interface circuit having a completion bit that indicates in alternate states that (a) a processor is finished with a current transfer to the interface circuit and (b) the interface circuit is ready to begin a new operation, as presently claimed. Claims 10 and 11 provide similar language. As such, the claimed invention is fully patentable over the cited references and the rejections should be withdrawn.

Claims 2-7, 9, 12, 14, 15 and 17-21 depend from claim 1, which is now believed to be allowable. As such, the dependent claims are fully patentable over the cited references and the rejections should be withdrawn.

The allowable matter of claim 15, along with base claim 1 and intermediate claims 12, 13 and 14, have been rewritten into independent form as new claim 22. As such, claim 22 is fully patentable over the cited references and should be allowed.

Language similar to the allowable matter of claim 15 including the intermediate claims 12, 13 and 14 have been written as dependent claims 23 and 24. As such, claims 23 and 24 are fully patentable over the cited references and should be allowable.

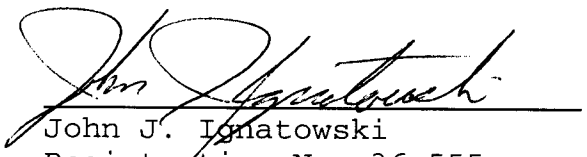
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative between the hours of 9 a.m. and 5 p.m. ET at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



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Dated: September 11, 2007

c/o Lloyd Sadler
LSI Corporation

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